REMARKS

Applicants respectfully request reconsideration of the present application in view of the foregoing amendments and in view of the reasons that follow.

Claims 11-13 and 22 are cancelled without prejudice.

Claims 21-23 are currently being amended. No new matter is added.

This amendment adds, changes and/or deletes claims in this application. A detailed listing of all claims that are, or were, in the application, irrespective of whether the claim(s) remain under examination in the application, is presented, with an appropriate defined status identifier.

After amending the claims as set forth above, claims 1-4, 9-10, 15-17, 19-21 and 23 remain pending in this application.

In paragraphs 1 and 2 of the Office Action, claims 21-23 are objected under 35 U.S.C. § 112, second paragraph for indefiniteness. Applicants have amended claims 21 and 23 in accordance with the Examiner's comments. Claim 22 has been cancelled. Entry of the amendment is respectfully requested because the amendment reduces issues for appeal. Accordingly, withdrawal of the rejection of claims 21 and 23 is respectfully requested. The amendments to claims 21-23 are made in a non-limiting fashion and are made for clarity.

In paragraphs 3-4 of the Office Action, claims 1-3, 11-13, 15-17 and 19-23 are rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,688,704 (Liu). The Examiner states:

> Re claim 1, Liu discloses a method for forming an IC, which comprises providing a gate dielectric layer 29 (fig. 5) above a top surface of a substrate 11; providing a silicon and nitrogen containing layer 17 (i.e., silicon nitride layer) above the gate

> dielectric layer (fig. 5); providing an oxide layer 19 above the silicon and nitrogen containing layer (fig. 2); selectively etching the oxide layer to form a first trench in the oxide layer (fig. 4); selectively etching the silicon and nitrogen containing layer to form a second trench (fig. 3) in the silicon and nitrogen containing layer, the second trench being narrower than the first trench and being disposed below the first trench (fig. 4); and providing a gate conductor material 31 in the first trench and the second trench to form the T-shaped gate conductor (fig. 5), see figs. 1-7 and cols. 1-4 for more details . . .Re claims 21-23, due to 112 problems, as best can be understood by the examiner is as following: the dielectric layer 19 (fig. 2) is silicon dioxide (col. 2, lines 35-40).

Applicants respectfully traverse the rejection.

In paragraphs 5, 6 and 7 of the Office Action, claims 4 and 9-10 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Liu. The Examiner states:

> Liu disclosed above, however, Liu does not explicitly show the width for the first and second trenches as shown in the instant claims 9-10 and using polishing process as shown in claim 4.
>
> It is well known in the art to use polishing process or etch-back process for planarization since both of them provide the same results. Therefore, it is obvious to one having ordinary skill in the art at the time the invention was made to either one of them.
>
> Furthermore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the method of Liu by selecting the suitable width for the first and second trenches, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 220 F.2d. 454, 456, 105 USPQ 233, 235 (CCPA 1955).

Applicants respectfully traverse the rejection.

On pages 5 and 6 of the Office Action, the Examiner responds to the arguments filed March 3, 2004. The Examiner states:

> Applicant stated that the instant claims 1 and 15 recites that the silicon and nitrogen containing layer is provided above the gate dielectric layer is noted. The prior art also shows this feature (i.e., fig. 5, the silicon nitride layer 17 is provided above the gate dielectric layer 29). Note: this layer (silicon and nitrogen containing layer) does not require to be in direct contact with the gate dielectric layer as shown in the claims. Furthermore, the claims fail to claim the sequential steps for forming the device (i.e., the term "comprising" indicates that the claim is open-ended and allows for additional steps).
>
> Applicant argues that the prior art requires an additional step not required by the instant invention. However, it is noted that the term "comprising" is used (open-end).
>
> Applicant request the examiner to provide a reference for the instant claim 4 is noted. For example, Lur et al., U.S. /5,981,383 teaches using polishing process or etch-back process for planarization, see col. 7, line 9-22

Applicants respectfully traverse the rejection.

In particular, Applicants traverse the Examiner's statement that the claims fail to recite the sequential steps for forming the device. Applicants respectfully submit that language in the claims inherently requires particular formation steps to occur in a particular order. For example, claim 1 recites:

> providing a gate dielectric layer above a top surface of the device and providing a silicon and nitride containing layer above the gate dielectric layer. (Emphasis Added).

Accordingly, claim 1 requires that the silicon and nitrogen containing layer be provided above the gate dielectric layer. Claim 15 includes similar explicit language.

Although the word "comprising" is an open-ended term, the silicon and nitrogen containing layer has to be provided above the gate dielectric layer because claim 1 explicitly states this requirement. If the gate dielectric layer is not there, it is impossible to provide the silicon and nitrogen containing layer above it. Claim 15 includes similar explicit language.

Therefore, pending independent claims 1 and 15 each require that the silicon and nitrogen containing layer be provided above the gate dielectric.

As discussed in the previous response to the Office Action, Liu discloses a conventional process in which a sacrificial layer is first provided above the substrate. The nitride layer is provided above the sacrificial layer and therefore is not provided above the gate dielectric layer as required by claim 1. Similarly, Liu does not disclose or suggest providing the first layer above the gate dielectric as required by claim 15. In fact, at no point in the process of Liu is the nitride layer provided above the gate dielectric layer. The gate dielectric layer is provided in an aperture in the nitride layer, a very different process from that recited in claims 1 and 15. Accordingly, it is respectfully submitted that independent claim 1 and its dependent claims 2-4, 9-10 and 21 and independent claim 15 and its dependent claims 16-17 and 19-20 and 23 are patentable over the cited art.

* * * * *

Applicants believe that the present application is now in condition for allowance. Favorable reconsideration of the application as amended is respectfully requested.

The Examiner is invited to contact the undersigned by telephone if it is felt that a telephone interview would advance the prosecution of the present application.

Atty. Dkt. No. 039153-0363 (F0804)

The Commissioner is hereby authorized to charge any additional fees which may be required regarding this application under 37 C.F.R. §§ 1.16-1.17, or credit any overpayment, to Deposit Account No. 06-1447. Should no proper payment be enclosed herewith, as by a check being in the wrong amount, unsigned, post-dated, otherwise improper or informal or even entirely missing, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 06-1447. If any extensions of time are needed for timely acceptance of papers submitted herewith, Applicants hereby petition for such extension under 37 C.F.R. §1.136 and authorizes payment of any such extensions fees to Deposit Account No. 06-1447.

Respectfully submitted,

Date 3-4-05

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